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EXAMINER	
SCHWARTZ, DARREN B	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/529,164	ITO, OSAMU	
	Examiner	Art Unit	
	DARREN SCHWARTZ	2435	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 10-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant amends claims 10 and 15.

Claims 1-7 and 10-15 are presented for examination.

Response to Arguments

Applicant's arguments filed with respect to claims 1-7 have been fully considered but they are not persuasive.

1. Applicant argues on page 8 of Remarks, "Initially, it is noted that the Examiner appears to rely on two different elements for the switching means of claim 1----that is, switching circuit 2 of Hirade and element (or switch) 130 of Fig.2 of Iyer."

The Examiner conquers with the assessment of the application of the applied combination of references, e.g. Hirade and Iyer.

Yet the Examiner reminds applicant the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981) and applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

2. Applicant argues with respect to claim 1 on page 9 of Remarks, "With regard to Hirade, the switching circuit 2 of Hirade does not appear to be supplied with scramble-processed data and does not appear to select the scramble-processed data when synchronization processing of transmit data is not performed."

The Examiner disagrees. Hirade clearly states "Figure 1 is a block diagram illustrating the sender side. Here, the pseudo random signal generator comprises tandom connected section (1) of 6 sections of shift registers SR1-SR6, and switching circuit (2) that selectively switches the feedback path of said tandem connected (1)." This is essentially verbatim.

3. Applicant argues with respect to claim 1 on page 9 of Remarks, "With regard to Iyer, the switch 130 of Iyer also does not appear to be supplied with scramble-processed data and, as such, does not appear to select the scramble-processed data when synchronization processing of transmit data is not performed."

The Examiner notes Iyer is introduced as teaching: "supplying the generated bit data of the predetermined pattern to one or more of the shift registers (Fig 2: col 4, lines 13-17) and for outputting the generated bit data of the predetermined pattern (col 1, lines 8-13; col 4, lines 60-61); the generated bit data of the predetermined pattern supplied to the one or more of the shift registers [Fig 2, elt 110] is the same as the generated bit data of the predetermined pattern supplied [Fig 2, elt "INPUT SEQUENCE"] to the switching means [Fig 2, elt 130] (Abstract; col 4, lines 23-29 and lines 42-47)."

Applicant's arguments with respect to claims 10-15 have been considered but are moot in view of the new ground(s) of rejection.

The fact that the Examiner may not have specifically responded to any particular arguments made by Applicant and Applicant's Representative, should not be construed as indicating Examiner's agreement therewith.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirade, Junji et al (JP 02249333), hereinafter referred to as Hirade, in view of Iyer et al (U.S. Pat 4713605 A), hereinafter referred to as Iyer.

Re claim 1: Hirade teaches a data processing apparatus adapted for performing scramble processing of transmit data (page 3: lines 1-2 of section "Problems to be solved by the invention") the data processing apparatus comprising:

scramble operation processing means including plural stages of shift registers (page 4: lines 1-4 of section "Means to solve the problems"), and a cyclic operation processing circuit for performing a predetermined operation processing on the basis of a hold value of a predetermined stage of the shift registers and the transmit data to

generate scramble-processed data (page 4: lines 6-9 and lines 12-13 of section “means to solve the problems”);

data generating means for generating bit data of a predetermined pattern (page 4: line 4 of section “Means to solve the problems;" page 5, lines 1-3 of section "Operation").

switching means supplied with the scramble-processed data and the bit data of the predetermined pattern generated by the data generating means to select the bit data of the predetermined pattern at the time of synchronization processing of transmit data (page 6: lines 3-5 of section "Application examples;” page 8, lines 3-5), and to select the scramble-processed data when synchronization processing of transmit data is not performed to output the data thus selected as scrambler output data (page 7, lines 1-7).

However, Iyer teaches supplying the generated bit data of the predetermined pattern to one or more of the shift registers (Fig 2: col 4, lines 13-17) and for outputting the generated bit data of the predetermined pattern (col 1, lines 8-13; col 4, lines 60-61).

the generated bit data of the predetermined pattern supplied to the one or more of the shift registers [Fig 2, elt 110] is the same as the generated bit data of the predetermined pattern supplied [Fig 2, elt “INPUT SEQUENCE”] to the switching means [Fig 2, elt 130] (Abstract; col 4, lines 23-29 and lines 42-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Hirade with the teachings of Iyer, for the purpose of providing checking and generating pseudo-random signals.

Additionally, Iyer provides a dynamic switching means of altering the input of a second LFSR. Both references are within the realm of applicant's invention as both teach generation of pseudo-random sequences using shifting registers.

Re claim 2: The combination of Hirade and Iyer teaches the data generating means is caused to be of the configuration to load the bit data of the predetermined pattern into the shift register at the time of synchronization processing of transmit data (Hirade: page 5: lines 8-11 of section "Operation;" page 6, lines 3-15).

Re claim 5: Hirade teaches a data processing apparatus adapted for performing scramble processing of transmit data (page 3: lines 1-2 of section “Problems to be solved by the invention”), the data processing apparatus comprising:

cyclic code generating means for generating cyclic bit data train of a predetermined period (page 4: lines 6-9 and lines 12-13 of section “means to solve the problems” and page 5: lines 1-3 of section “Operation”),

EXOR operation means for sequentially performing EXOR operation of the cyclic bit data train with respect to the transmit data to output scramble-processed data (page 6, line 10 through page 7, line 7);

data generating means for generating bit data of a predetermined pattern (page 4: line 4 of section “Means to solve the problems;" page 5, lines 1-3 of section "Operation"); and

However, Iyer teaches supplying the generated bit data of the predetermined pattern to the cyclic code generating means (Fig 1: col 2, lines 27-29 and col 4, lines 13-

17) and for outputting the generated bit data of the predetermined pattern (col 1, lines 8-13; col 4, lines 60-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Hirade with the teachings of Iyer, for the purpose of providing generating and outputting long-pseudorandom sequences. Both references are within the realm of applicant's invention as both teach generation of pseudo-random sequences using shifting registers.

The combination of Hirade and Iyer teaches switching means supplied with the scramble-processed data from the EXOR operator means and bit data of a predetermined pattern generated by the data generating means to select the bit data of the predetermined pattern at the time of synchronization processing of transmit data (Hirade: page 6: lines 3-5 of section "Application examples;" page 8, lines 3-5; Iyer: Fig 1, elt 28; Fig 2, elts 110, 130 & 120; the Examiner notes the switching means of Iyer, e.g. Fig 2, elt 130, switches data between INPUT SEQUENCE and DATA OUT of which the DATA OUT sends data from DATA IN which contains Fig 2, elt 28, e.g. XOR gate), and to select the scramble-processed data when synchronization processing of the transmit data is not performed to output the data thus selected as scrambler output data (Hirade: page 7, lines 1-7).

The combination of Hirade and Iyer further teaches the generated bit data of the predetermined pattern supplied to the cyclic code generating means [Fig 2, elt 110] is the same as the generated bit data of the predetermined pattern supplied Fig 2, elt

“INPUT SEQUENCE”] to the switching means [Fig 2, elt 130] (Abstract; col 4, lines 23-29 and lines 42-47).

Re claims 3 and 6: The combination of Hirade and Iyer teaches the switching means is caused to be of the configuration in which in the case where a predetermined synchronization pattern data inserted into the transmit data for the purpose of taking synchronization of the transmit data is inserted in the transmit data, the switching means serves to select the bit data of the predetermined pattern to output the bit data thus selected as scrambler output data (Hirade: page 5: lines 8-11 of section "Operation;" page 6, lines 3-15).

Re claims 4 and 7: The combination of Hirade and Iyer teaches the data generating means is caused to be of the configuration to generate bit data of a predetermined pattern to which predetermined information is assigned in advance (Hirade: page 3-4, entire section: ”problems to be solved by the invention”).

5. Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Padovani et al (U.S. Pat 5535239 A), hereinafter referred to as Padovani, in view of Ziolko et al (U.S. Pat 4827514 A), hereinafter referred to as Ziolko, in further view of Schroeder (U.S. Pat 3784743 A), hereinafter referred to as Schroeder.

Re claim 10: Padovani teaches a data processing apparatus adapted for performing scramble processing of transmit data, the data processing apparatus comprising: a random number generating circuit to generate a random bit data train, said random number generating circuit having a first shift register, a second shift

register, and a first adder, said random number generating circuit being arranged such that (i) an output stage of the first shift register is coupled to an input stage of the second shift register and to the first adder, and (ii) an output stage of the second shift register is coupled to the first adder (see Figure 3: associated elts of 62, 64 & 66);

a data generator to generate bit data of a predetermined pattern and to supply the generated bit data of the predetermined pattern therefrom (col 13, lines 3-14), said data generator being separate from the random number generating circuit (Fig 1, elts: "SECONDARY TRAFFIC DATA," 30, 46 & 60).

Ziolko teaches a first switch arranged to receive the scramble-processed data from the second adder and the bit data of the predetermined pattern from the data generator , said first switch being operable to select the bit data of the predetermined pattern at the time of synchronization processing of the transmit data and to select the scramble-processed data when synchronization processing of the transmit data is not performed and to output the data selected (Fig 1, elts 100, 102, 106 & 108: col 2, lines 28-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Padovani with the teachings of Ziolko, for the purpose of providing a secure synchronous communications systems. Both references are within the same field of endeavor of securing data signals.

However, the combination of Padovani and Ziolko do not expressly disclose that during operation an output from the first shift register is supplied to the input stage of the

second shift register and to an input of the first adder and during operation an output of the second shift register is supplied to another input of the first adder.

Schroeder teaches that during operation an output [Fig 1, elt 25] from the first shift register [Fig 1, elt 23] is supplied to the input stage [Fig 1, elt 25] of the second shift register [Fig 1, elt 27] and to an input of the first adder [Fig 1, elt 30] and during operation an output of the second shift register [Fig 1, elt 27] is supplied to another input of the first adder [Fig 1, elt 30] (col 3, lines 20-21; col 3, lines 28-31; col 3, lines 58-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Padovani and Ziolko with the teachings of Schroeder, for the purpose of expeditiously generating pseudorandom signals via reentrant shift registers with feedback, as taught by Schroeder.

Re claim 11: The combination of Padovani, Ziolko and Schroeder teaches the data generator is further arranged to supply the generated bit data of the predetermined pattern to the first shift register and the second shift register (Fig 3, see the two LSR's), and in which said random number generating circuit is further arranged such that the output of the first adder is supplied to an input stage of the first shift register (Fig 3, see top LSR outputs to XOR and feedbacks into top LSR), and in which the generated bit data of the predetermined pattern supplied to the first switch is the same as the generated bit data of the predetermined pattern supplied to the first shift register and the second shift register (Padovani: Fig 3, elts 60 and shift registers; Ziolko: Fig 1, elts 100, 102, 106 & 108: col 2, lines 28-48).

Re claim 12: The combination of Padovani, Ziolko and Schroeder teaches the first adder is a modulo 2 adder, and in which the first adder and the second adder are each operable to perform an exclusive-or operation (Padovani: 55-62).

Re claim 13: The combination of Padovani, Ziolko and Schroeder teaches a second switch arranged to receive the output of the first adder and the bit data of the predetermined pattern and being operable to output a selected one of the output of the first adder and the bit data of the predetermined pattern to an input stage of the first shift register (Fig 3, see bottom LSR outputs to XOR and feedbacks into bottom LSR) and in which the generated bit data of the predetermined pattern supplied to the first switch is the same as the generated bit data of the predetermined pattern supplied to the second switch (Padovani: Fig 3, elts 60 and shift registers; Ziolko: Fig 1, elts 100, 102, 106 & 108: col 2, lines 28-48).

Re claim 14: The combination of Padovani, Ziolko and Schroeder teaches the first adder is a modulo 2 adder, and in which the first adder and the second adder are each operable to perform an exclusive-or operation (Padovani: 55-62).

Re claim 15: Claim 15 is rejected under similar grounds as those provided in claim 10.

Conclusion

Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to

specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the text of the passage taught by the prior art or disclosed by the examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DARREN SCHWARTZ whose telephone number is (571)270-3850. The examiner can normally be reached on 7am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on (571)272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. S./
Examiner, Art Unit 2435
/Kimyen Vu/
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